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**1005**

Lab Activity-April 6, 2020- 8:1 mux.

Deadline: Sunday April 12, 11:59 PM

Each student must submit individually the text editor, output editor, and the Schematics regarding VHDL Coding for one of the following digital circuit:

The Big Group ONE:

8:1 MUX

The Big Group TWO:

1:8 DEMUX

**Code:-**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity mux\_8\_1 is

Port ( d : in STD\_LOGIC\_VECTOR(7 DOWNTO 0);

s : in STD\_LOGIC\_VECTOR (2 downto 0);

STRBbar : in STD\_LOGIC;

Output : out STD\_LOGIC);

end mux\_8\_1;

architecture Behavioral of mux\_8\_1 is

begin

process(STRBbar,d,s)

begin

if (STRBbar = '0') then

case s is

when "111" =>output<=d(7);

when "110" =>output<=d(6);

when "101" =>output<=d(5);

when "100" =>output<=d(4);

when "011" =>output<=d(3);

when "010" =>output<=d(2);

when "001" =>output<=d(1);

when others =>output<=d(0);

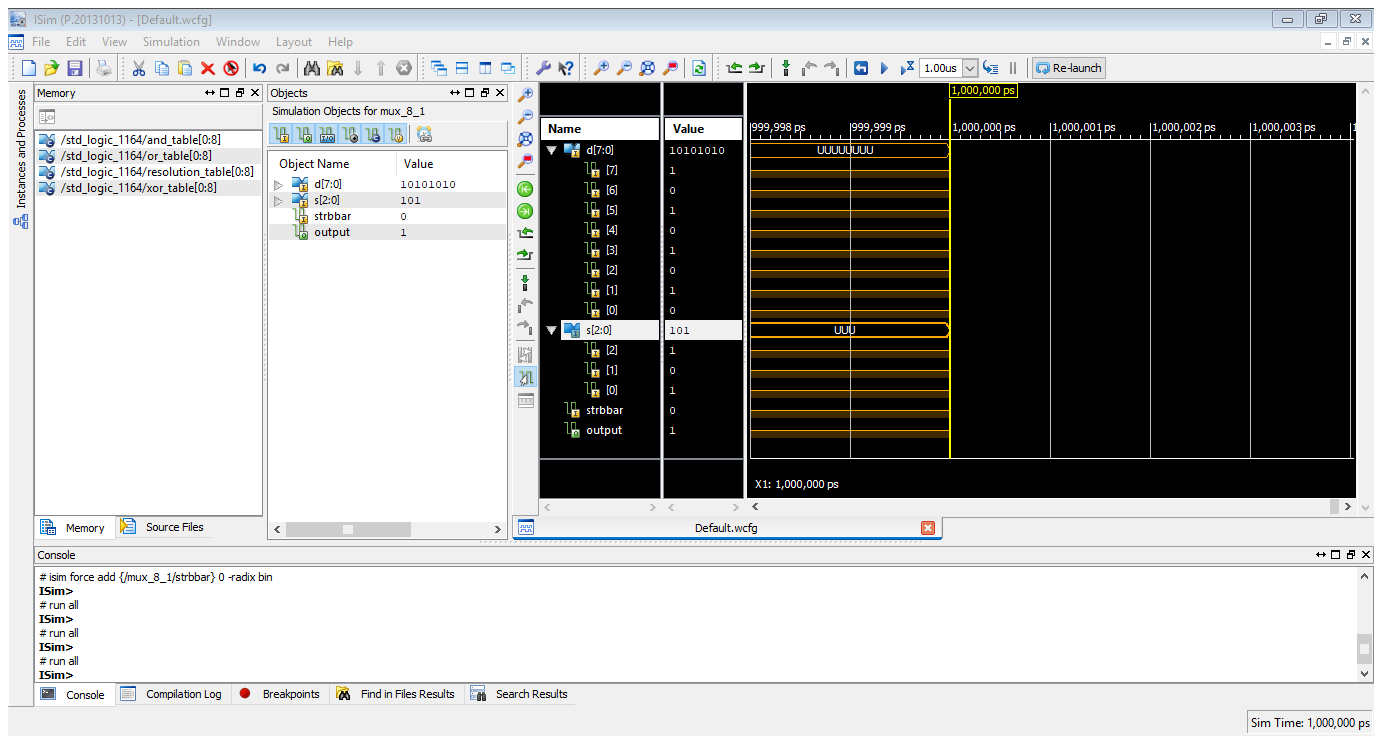
end case;

end if;

end process;

end Behavioral;

Output:-



Schematic:-

